Agilent Technologies

Logic Analysis Basics

February 11, 2003

presented by:

Sarah Herron

Introduction

If you have ever asked yourself these questions:

- What is a logic analyzer?
- What is a timing/state analyzer?
- What is a trigger?
- When should I use a logic analyzer?

Then you are in the RIGHT place!!!

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Agenda

- **Overview of a Logic Analyzer**
- **Logic Analyzer Process**
  - **Connect (Probing)**
  - **Acquire**
    - **Timing Analyzer**
    - **State Analyzer**
  - **Data Analysis Tools and Display**
- **Conclusion**

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Logic Analyzer is a Tool that:

Gives you insight into the operation of a *digital* circuit by

- Connecting to your DUT (Device Under Test)

- Capturing and storing the digital waveforms

- Analyzing the stored data and displaying the results.

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What Can a Logic Analyzer Do for Me?

- **Record a circuit's logic levels over time, and let you examine the record**
- **Show whether or not a particular event happens (the trigger)**
- **Provide a precise measure of time between events**
- **Inverse-assemble a microprocessor's logic levels to tell you what code was running**
- **Analyze complex buses and protocols**

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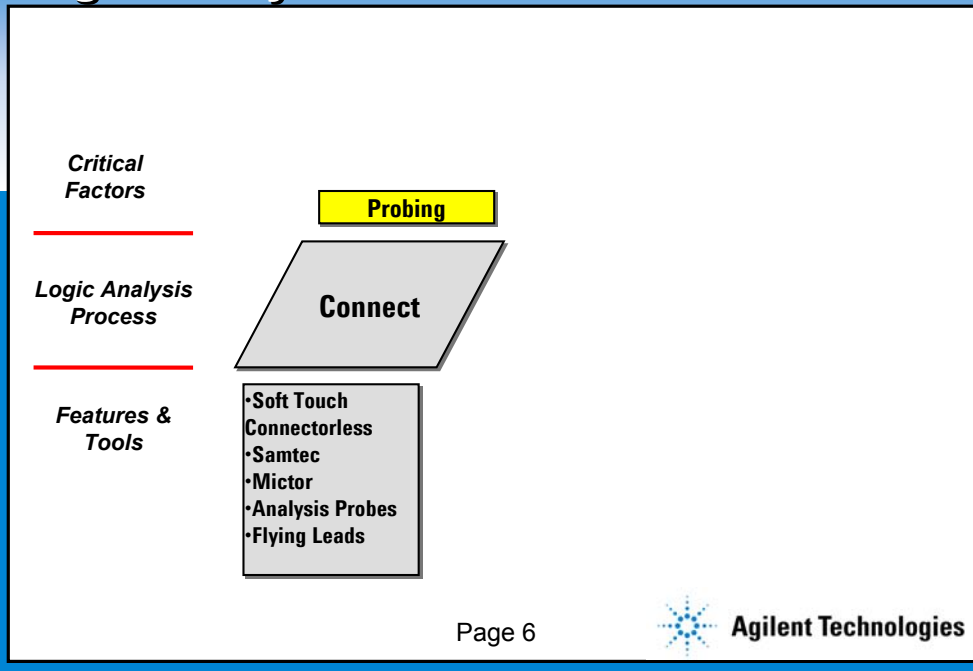**You should use a logic analyzer:**

-When you need to see many signals at once.

-When you need to look at signals in your system the same way your hardware does.

-When you need to trigger on a pattern of highs and lows on several lines and see the results.

-When you need to monitor the behavior of complex systems including HW/SW integration

Logic Analysis Process

Critical Factors

Logic Analysis Process

Features & Tools

Probing

Connect

- Soft Touch Connectorless
- Samtec
- Mictor
- Analysis Probes
- Flying Leads

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Logic Analysis has always been positioned for consideration in terms of the 'banner specifications' of Acquisition speed, memory depth, and channel count. Of course these are still very important. If it is not fast enough, deep enough, or wide enough to capture your data, there is no point considering it further.

But once you move beyond those specs, you must still consider the solution as a whole. Many of the 'details' can make or break your ability to debug your system.

Let's run through some critical factors for consideration….

First, you have the probing problem and if you don't get this done right, the rest of the process is at risk. Probing comprises the Connection part of the process and Agilent offers a variety of solutions to meet your needs.
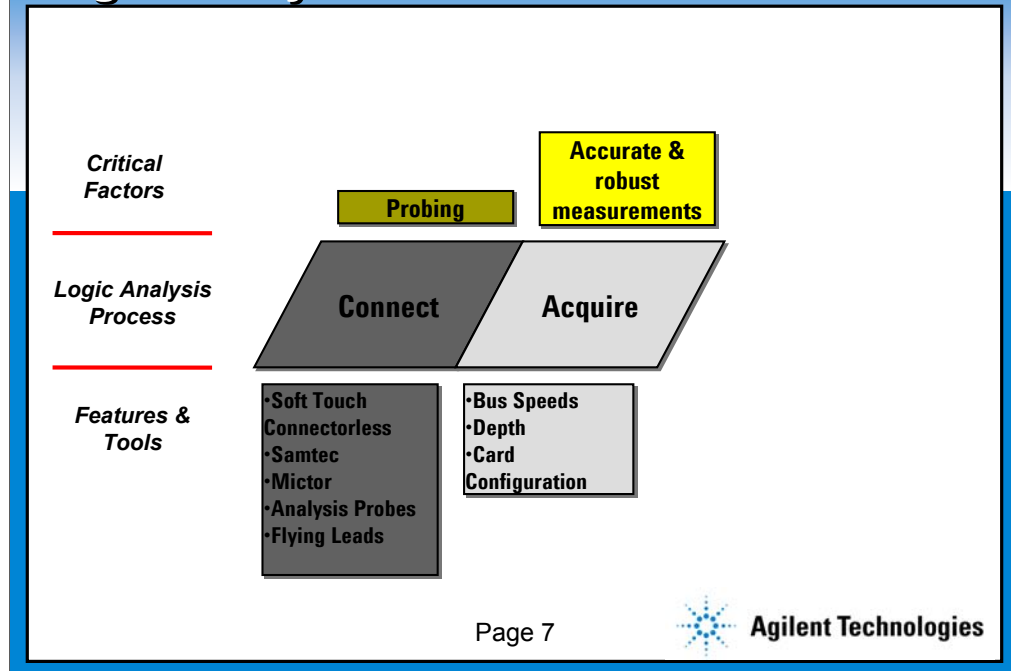
The second consideration is how you are going to make accurate and robust measurements. This is the Acquire part of the process and there are a variety of solutions to meet different needs.

Finally, you have to analyze the data, and insome cases, this requires additional insight into signal integrity. This is the Present data phase and there are a variety of ways to look at the acquired data.

CONNECT-ACQUIRE-PRESENT – If you think about your logic solution in terms of this model you can begin to see the big picture that goes beyond banner specs.

The rest of our slides will walk through each of these steps and show you some things that Agilent believes truly add unique value and when combined, offer an unparalleled solution.

Logic Analysis Process

Critical Factors	**Probing**	**Accurate & robust measurements**
Logic Analysis Process	**Connect**	**Acquire**
Features & Tools	•Soft Touch Connectorless •Samtec •Mictor •Analysis Probes •Flying Leads	•Bus Speeds •Depth •Card Configuration

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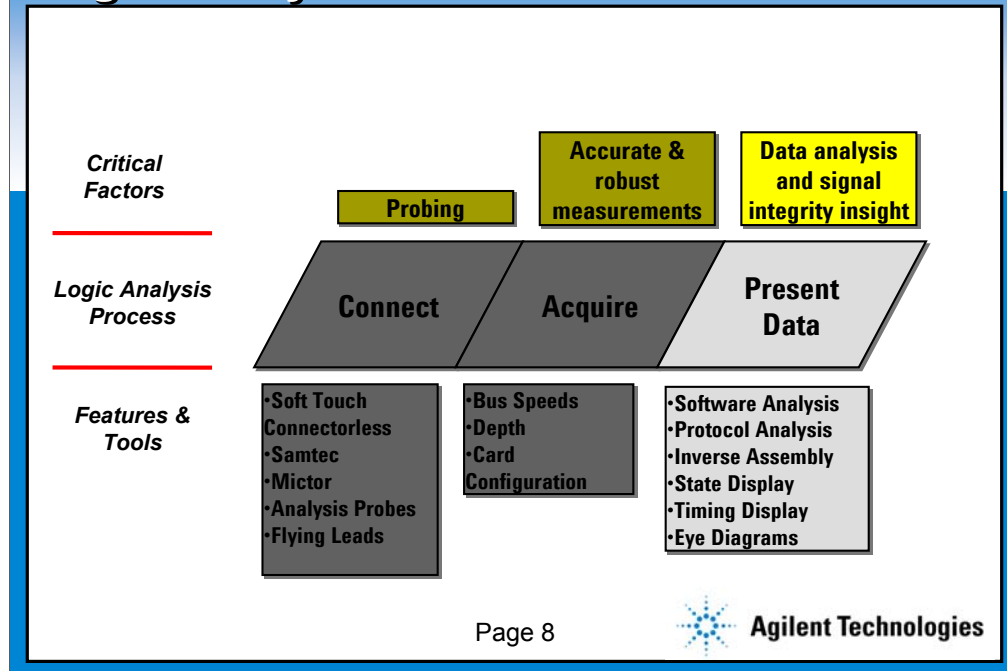
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Logic Analysis Process

Critical Factors		Probing	Accurate & robust measurements	Data analysis and signal integrity insight

Logic Analysis Process

Connect / Acquire / Present Data

Features & Tools

•Soft Touch Connectorless •Samtec •Mictor •Analysis Probes •Flying Leads	•Bus Speeds •Depth •Card Configuration	•Software Analysis •Protocol Analysis •Inverse Assembly •State Display •Timing Display •Eye Diagrams

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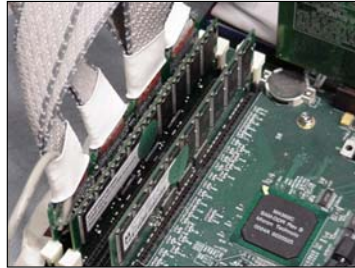
It Begins At The Probe…

General-purpose probing

Designed into the target

✴ Agilent

Application-specific probes

✴ **Agilent Technologies**

Let's start with the connection phase…

You must get probing right if want to make dependable measurements. It starts there and it can be the limiting factor in your ability to acquire data if it is not done properly. Probing is not an easy decision because it is often about the tradeoffs that must be made around its electrical and mechanical impact on your system. You can not escape the fact that probing is invasive but you can minimize how invasive it is.

What kind of probe you need depends on what you're making measurements on. In many cases you need to attach probes to buses or signals directly on your PC board. in other cases, Agilent and our premier solution partners provide what we call analysis probes, which are tailored to the needs of a specific interconnect standard. The one shown on the right is a DDR memory probe

Today we will concentrate on the first two - particularly the recent innovations in connectorless probing for general purpose applications.

Electrical Probing Considerations

- **How can I connect to my signals?**
  - **Design-in connector**
  - **Flying leads**
- **Low loading**
  - **System tolerance**
  - **Impact on DUT**

Connect / Acquire / Present

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Lets first take a step back and think about probing in a more general sense. We believe that there are some very well defined factors that define a good probing solution and we have listed them here. I imagine if you were to define your perfect probe it would hit on all or most of these things.

In the past, we have always viewed the first 2 categories as 'musts' when it came to probe design. Of course there are always tradeoffs and a certain threshold of what is acceptable. There is no perfect probe.

The last category has always been the icing on the cake but users have been willing to compromise on these if it gets them to their data.
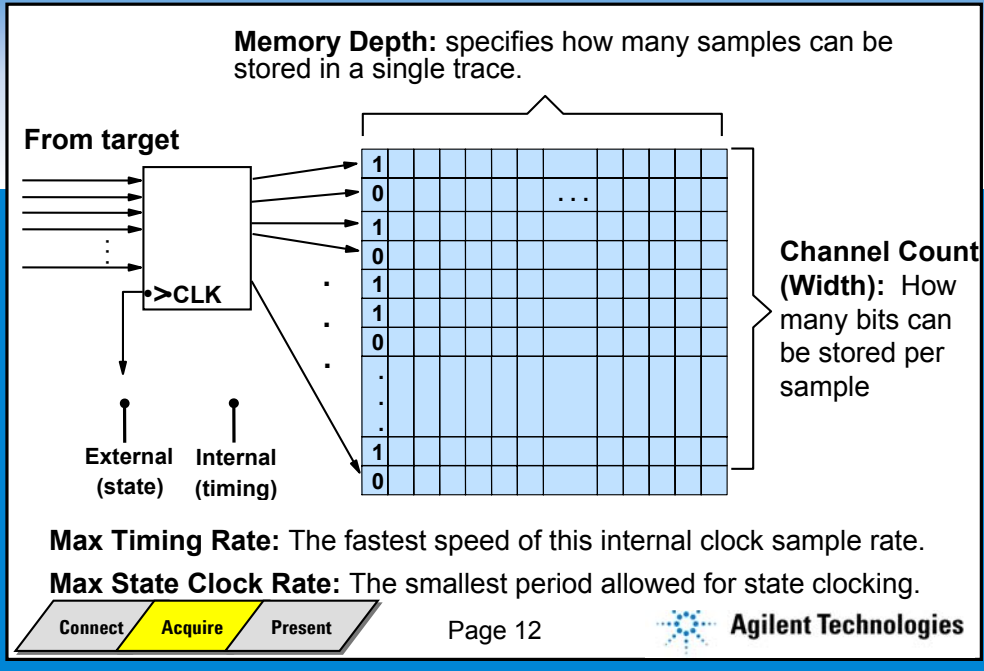
So why bring this up?

As probing technology advances, you hope to continually decrease the size and number of tradeoffs. Advancing technology demands this.

The latest innovations in gp probing revolve around the concept of 'Connectorless Probing' and this innovation is currently receiving a lot of attention as the superior approach to gp probing. Both Tek and Agilent are offering a connectorless solution but are using VERY different approaches. The old way, and the way Tek is currently doing it, is an elastomeric compression probe. Agilent's solution is what we consider to be a generation beyond elastomeric probing. We also believe it moves beyond some of the old tradeoffs you had to put up with.

Lets look at a little history around connectorless solutions…..

Mechanical Probing Considerations

- **What can I fit on my board?**
  - **Footprint size**
  - **Signal routing**
  - **Low profile**
- **Usable**
  - **Easy to attach**
  - **Reliable, repeatable**

Connect / Acquire / Present   Page 11   Agilent Technologies

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Memory Depth: specifies how many samples can be stored in a single trace.

From target

>CLK

External (state)   Internal (timing)

1 0 1 0 1 1 0 . . .
1 0

. . .

Channel Count (Width): How many bits can be stored per sample

Max Timing Rate: The fastest speed of this internal clock sample rate.

Max State Clock Rate: The smallest period allowed for state clocking.

Connect   Acquire   Present   Page 12   Agilent Technologies

The shaded area shown above represents the total, finite amount of logic analyzer memory. This memory may be distributed in various ways. When the analyzer is used in Full Channel mode, there is a maximum of 128M memory on each channel.

 The memory may be reduced at any time to speed up traces of infrequent events, if desired. Individual channel memory may also be doubled by switching to Half Channel mode (Timing mode only).

This redistributes the same amount of memory over half as many channels, doubling the number of samples/window of time that may be stored on remaining channels.

State measurements must be displayed in a format easy for the user to interpret and analyze. The logic analyzer can be programmed through a configuration menu to [highlight 1] group the measurement channel results under descriptive labels like [highlight 2] ADDR, DATA and STAT. These labels identify the measured states for the address, data and control busses, respectively. This configuration [show 3] is called the state format specification.

Acquire - Two Measurement Modes
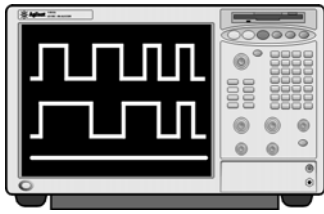
Timing Analysis

(Logic Timing)

State Analysis

1100101
0110011
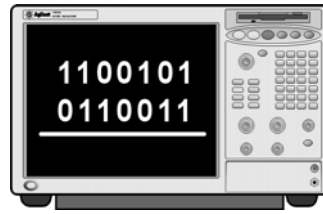
(Logic Events)

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Two types of measurements are performed in logic analysis: state and timing measurements. A logic analyzer contains both a state analyzer and a timing analyzer.

The state analyzer measures the occurrence of logic states or events and represents them as numbers.

The timing analyzer measures the timing of logic states or events and represents that information as waveforms.

Acquire - Two Measurement Modes
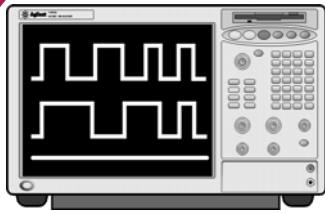
Timing Analysis

(Logic Timing)

1100101
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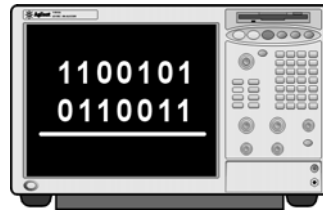
State Analysis

(Logic Events)

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Let's begin with a discussion of Timing Analysis

Timing Mode (Asynchronous)

Tells *when* the event happened

- **Display signal edge timing relationships**

- **Trigger across multiple channels**

- **Analogous to an oscilloscope with 1-bit resolution**

- **Useful for hardware debug**

Asynchronous – Sampling clock comes from internal logic analyzer

$V_{Threshold}$

V_{Input}

Output
(0 or 1)

$+$
$-$

Latch

V_{Output}

Comparator

Internal
Analyzer
Clock

V_{Input} $V_{Threshold}$

Internal
Analyzer
Clock

V_{Output}

Connect / Acquire / Present   Page 17   Agilent Technologies
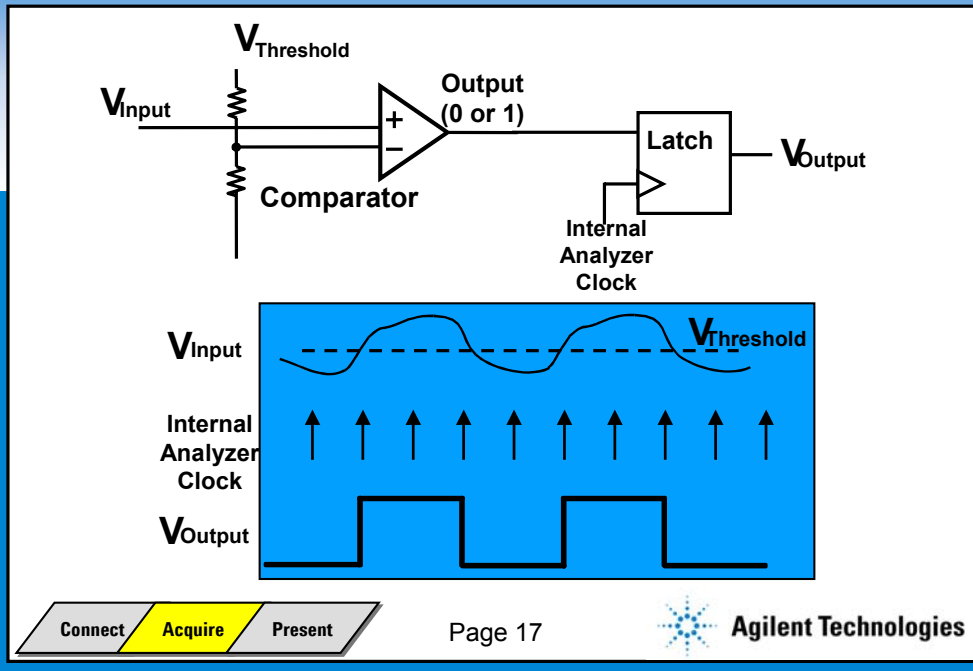
A timing analyzer is the part of a logic analyzer that is like a digitizing scope with one bit of vertical resolution and many channels. It displays information in the same general form as a scope, with the horizontal axis representing time and the vertical axis as voltage amplitude.

With one bit of resolution, you can display only two states – high or low. It samples data at regular time intervals using an internal clock.

This data is usually displayed in a waveform view similar to an oscilloscope. 0 represents below threshold and 1 represents above threshold. Because the waveform is time-dependant, the waveform display is said to be in the "time domain".

The output in timing mode is a square wave representing the value with respect to threshold of the signal at the time it was sampled (at each internal clock edge).

The comparator output provides a signal with stable voltage levels to the measurement channel. To digitize this signal a timing reference, or clock signal, is needed. The measurement channel uses a latch, and a clock signal from either the DUT or the logic analyzer to convert the comparator output to digital data.

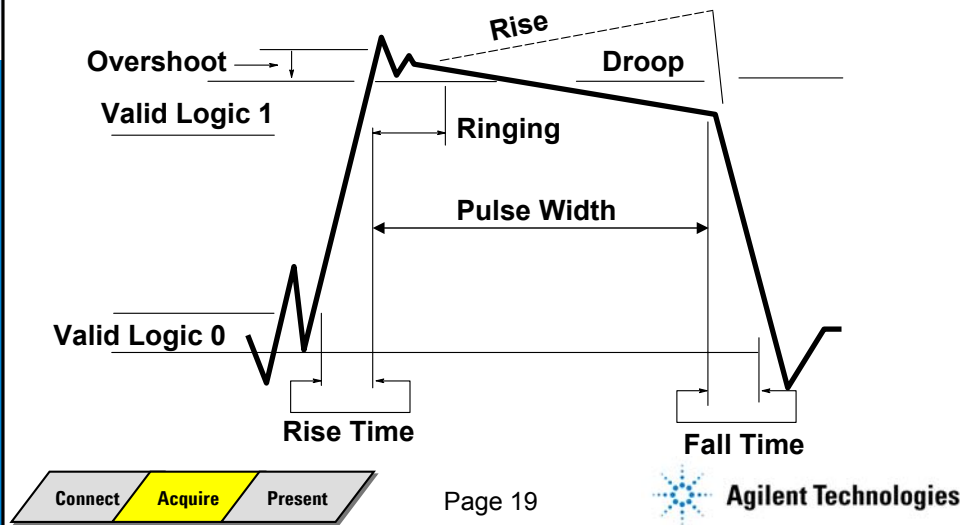# Timing Waveform

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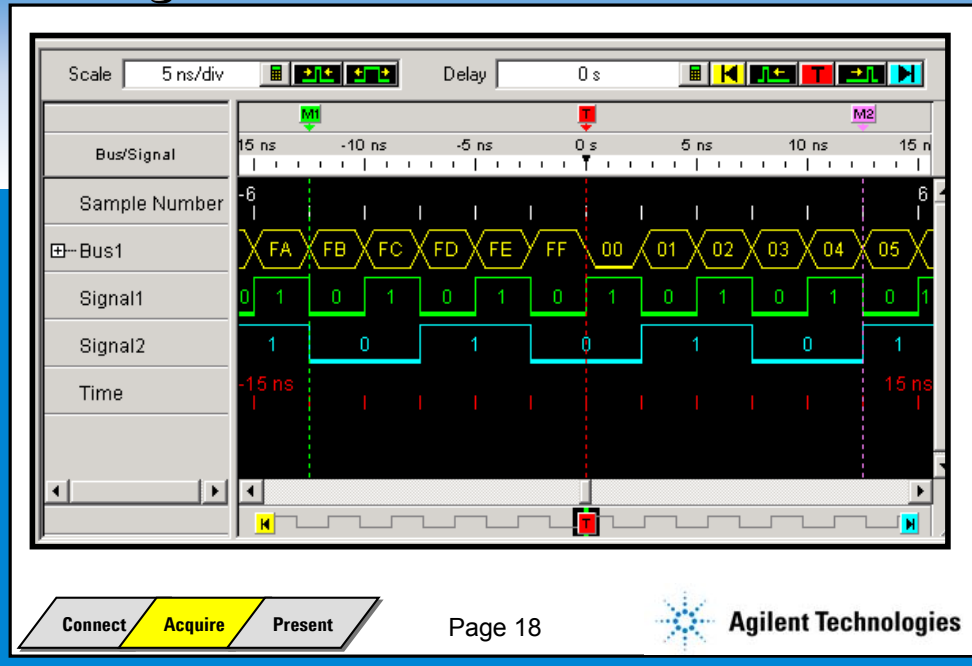
Each sample clock active edge, tells the analyzer when to acquire a sample. In timing mode, the sample clock comes from the logic analyzer module. In state mode, the sample clock is derived from the device under test, usually a bus clock.

The timing analyzer oversamples the signal much like an oscilloscope so that the device activity between states can be seen.

When to Use an Oscilloscope

- **Parametric Measurements**
- **Precise Time vs. Voltage Relationships**

Rise

Overshoot →

Valid Logic 1

Droop

Ringing

Pulse Width

Valid Logic 0

Rise Time

Fall Time

Since a logic analyzer only has one comparator per channel, it cannot faithfully reproduce a signal, it can only determine whether the signal at the time of sampling is above or below the threshold voltage. In order to take parametric measurements and accurately view signal characteristics, an oscilloscope must be used.

When to Use a Logic Analyzer

- **Cause and effect timing relationships**
- **Many channels simultaneously**
- **Multiple bus correlation measurements**

Connect / Acquire / Present

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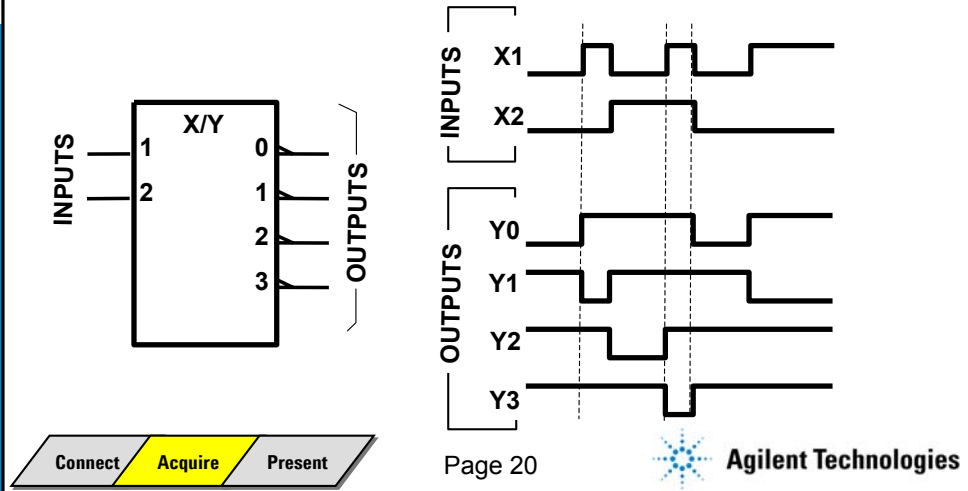
Timing analysis sacrifices the resolution of an oscilloscope in order to gain access to many channels simultaneously. The ability to monitor signals on all of the busses at any given time provides a clear picture of what is going on inside the microprocessor.

While scopes are usually limited to 4 channels, logic analyzers can probe, acquire and display 100s of channels simultaneously.

High Speed Timing Zoom

- **Efficiently characterize hardware with 250ps resolution**
- **Useful at high speeds**
- **Capture simultaneously with traditional timing or state measurements**
- **Provides a window of visibility around the trigger**

Up to 4 GHz timing speeds at 64k memory depth

Transitional Sampling

- **Only stores transitions**
- **Utilize memory efficiently**
- **Two memory locations per transition**

Signal being acquired

|← 200ns →| |← 10s →| |← 200ns →|

Sampling points   Memory Full
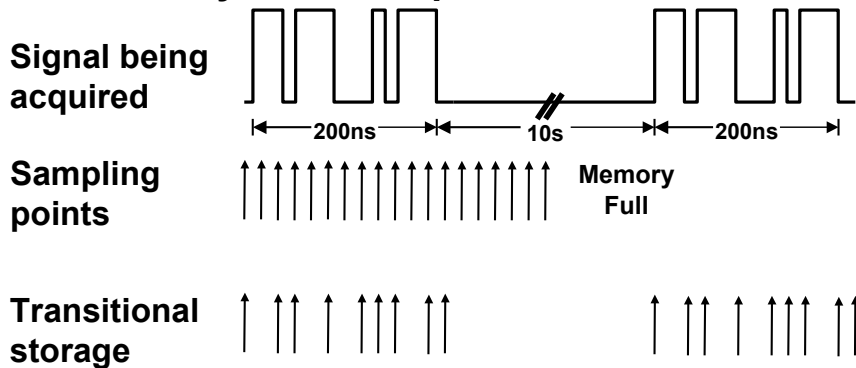
Transitional storage

Conventional mode is most effective for signals which transition frequently and/or which occur over a brief period of time.

With this mode, however , there is a trade-off between resolution and total acquisition time. Remember that every sampling point uses one memory location. Thus, the higher the resolution (faster sampling rate), the shorter the acquisition window.

Transitional sampling, makes more efficient use of memory by storing only those samples that were preceded by a transition, together with the elapsed time from the last transition. Thus we use only two memory location per transition and no memory at all if there is no change in activity.

In this example, we are sampling at 200MHz, or in 5ns increments. It would take 40 memory locations to store the initial burst of information. It would then take an additional 2 million memory locations to store the 10s of deadtime. Instead of wasting all of these locations, Transitional timing will only capture when there is a transition. This means only 2 storage positions are required for the entire 10s of deadtime.

Acquire - Two Measurement Modes
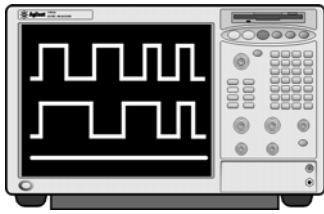
Timing Analysis

(Logic Timing)
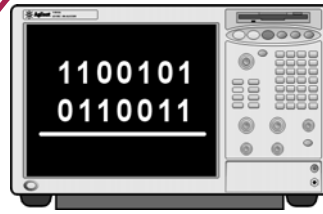
State Analysis

(Logic Events)

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Now let's switch gears and talk about State Analysis

State Analysis (Synchronous)

**Useful for determining *what* happened**

- **Trace values on a bus**
- **Track functional problems and code flow**
- **Useful for software debug and hardware/software integration**
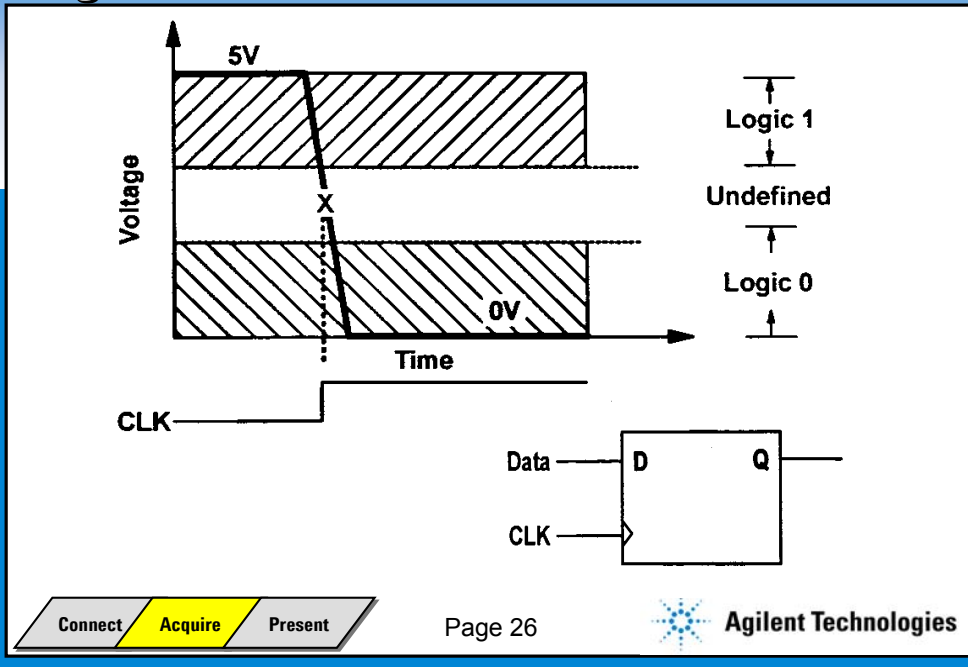
Synchronous – Sampling clock comes from device under test (DUT)

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Data Valid Window

- **Period of time in which data is stable**
- **Setup time – edge may be transitioning**
- **Hold time – data is stable**

Data is stable

Data is transitioning

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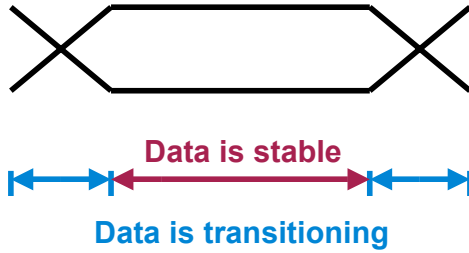
Edge Transitions

Setup time and hold time are important characteristics of digital devices. They are defined by the semiconductor manufacturer of the particular device.

For the D flip-flop to operate correctly, the D input must be stable at a valid logic level for a specific time before the rising clock edge. This time is called the setup time .

There may also be a requirement that the D input remain stable for short time after the clock edge. This time is called the hold time.

Why is setup and hold time important? Imagine what would happen if the clock edge occurred at the same time the data was switching through the undefined zone without the data being held stable for a fixed period.

In the example above, 5 V is high and 0 V is low. The voltage at the clock edge is in the undefined zone of voltages. At this voltages it is impossible to determine whether a logic 1 or a logic 0 is clocked into the flip-flop. It may be either.
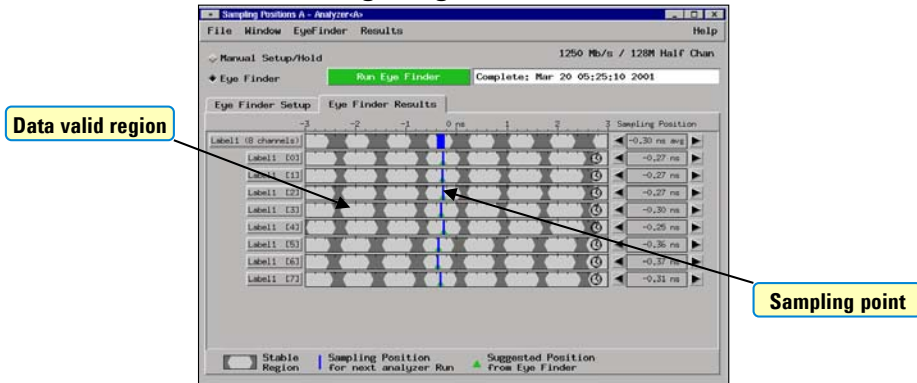
Setup and Hold Example

Hold Time

D Flip Flop

DUT Clock

Setup Time

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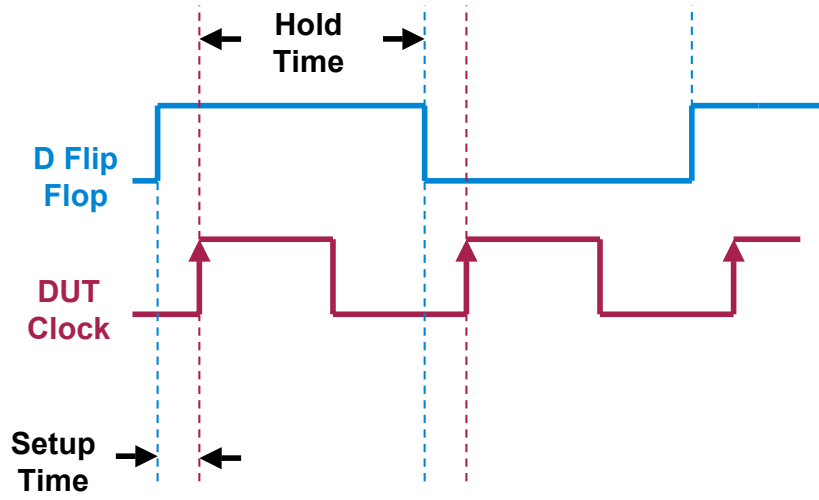
Eye Finder

Immediate confirmation and confidence in sampled data!

- **Automatic placement of sample position in the data valid region**
- **Easy to modify manually**
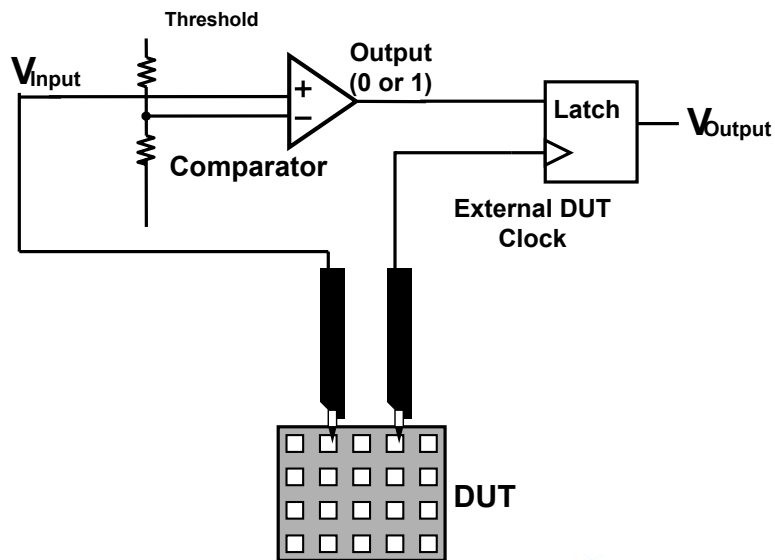- **Quick overview of target signal skew**

Data valid region

Sampling point

Connect / Acquire / Present Page 28 Agilent Technologies

Agilent takes the commitment to reliable measurements seriously. Agilent chose a simple, reliable sampling architecture for logic analyzers, and we provide you an indispensable aid for reliable state measurements: eye finder. Without going into too deep technical detail, the challenge is to find the center of the data valid eye for each signal coming into the logic analyzer; to set the sampling point to the center of the eye on each channel; and to make sure it stays there.

Eye finder examines the signals in your circuit for millions of clock cycles to find the data valid regions. In the eye finder display, the data valid regions are the clear regions. The sampling points selected by eye finder are indicated in blue.

The center of the screen (0 ns) corresponds to the clock.

Independent of the sample position setting, Eye Finder also provides a very fast view of target signal skew. If a particular signal in a bus   is skewed out of alignment with the rest of the bus, eye finder will show it. With older analyzers, this sort of problem would be effecting your data significantly and could be extremely difficult to find.

Synchronous Measurement

Threshold

V_{Input}

Output (0 or 1)

Comparator

Latch

V_{Output}

External DUT Clock

DUT

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In a synchronous measurement, a synchronizing signal is taken from the DUT and used by the measurement channel as a timing, or clock signal. The clock signal provides the timing information required to identify valid logic states of the DUT and convert them to data.

State Domain

DATA ⟨ AA ⟩⟨ 0C ⟩⟨ 61 ⟩⟨ B3 ⟩

CLOCK

Clock	Data
1	AA
2	0C
3	B3

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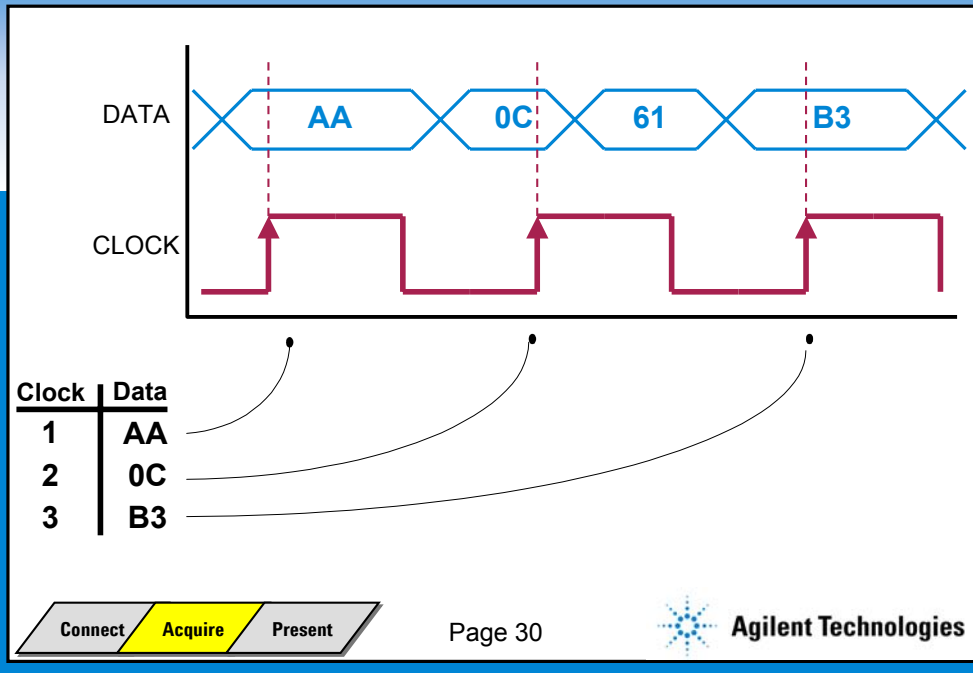
A state analyzer samples data based on an external clock .   Each time the state analyzer receives a qualified edge from the device under test (DUT), it samples and stores each input in the trace buffer. Data collected in this manner is typically displayed as a sequential list of logical states in a listing display.

State Listing

- Trace values on a bus (see data values your device sees)
- Track functional problems and code flow

Circuit

ADDR 16

CPU

DATA 8

MEMORY

STAT 8
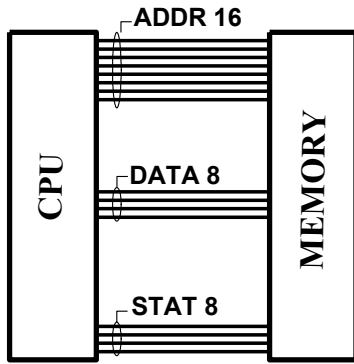
Measurement

Label>	ADDR	DATA	STAT
Base>	HEX	HEX	SYMB
-0003	0436	15	OPCOD
-0002	0BB6	04	MEMWR
-0001	0BB5	37	MEMWR
+0000	0024	C3	OPCOD
+0001	0025	00	MEMRD
+0002	0026	08	MEMRD
+0003	0008	22	OPCOD
+0004	0009	D3	MEMRD

Connect / Acquire / Present

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State analysis uses the clock on the device under test as the sampling clock. This means that data is only sampled when it is valid. The output in state mode is a listing of the values that crossed the bus, with the option of a time stamp noting when the values occurred.
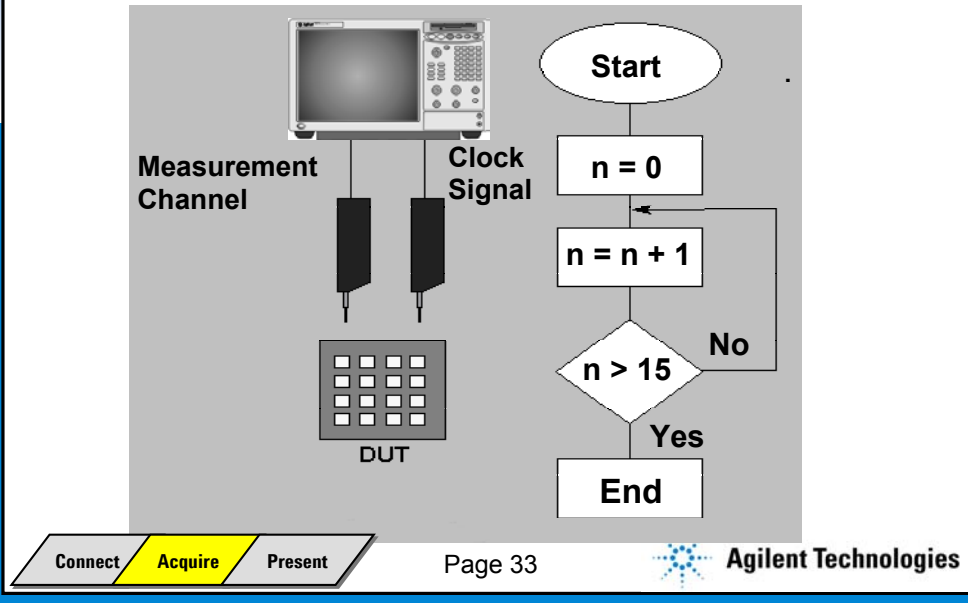
The logic analyzer can go even further with inverse-assembler capability, and display the actual assembly language code executed by the system. This allows the user to easily check the program code executed by the microprocessor.

State Analyzers

Ideal for Analyzing the Execution of Microprocessor Programs

Measurement Channel

Clock Signal

Start

n = 0

n = n + 1

n > 15

No

Yes

End

DUT

Connect | Acquire | Present

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State measurements are useful for monitoring and analyzing the execution of computer software programs. State analyzers are excellent tools to debug and optimize computer code.

State analyzers have sequence levels that aid triggering and storage. Sequence levels allow you to qualify data storage more accurately than a single trigger point. This means that you can more accurately window in on the data without storing information you do not need.

Sequence levels usually look something like this:

1 find XXXX else on XXXX go to level x

2 then find XXXX else on XXXX go to level X

3 trigger on XXXX

Sequence levels are especially useful for getting into a subroutine from a specific point in the program.

Rule of Thumb

- **Use a State Analyzer to see *what* happened on a bus**
- **Use a Timing Analyzer to see *when* it happened.**

Q&A

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Triggering

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The Conveyor Belt Analogy

Trigger Sample

Newest Sample

Stop

Oldest Sample

Trace Memory Depth

One Sample   = One box
Acquired Samples = Boxes on the belt
Memory Depth   = Number of boxes that will fit on the belt
Trigger Position   = Position of special box when Stop button
                               is pressed

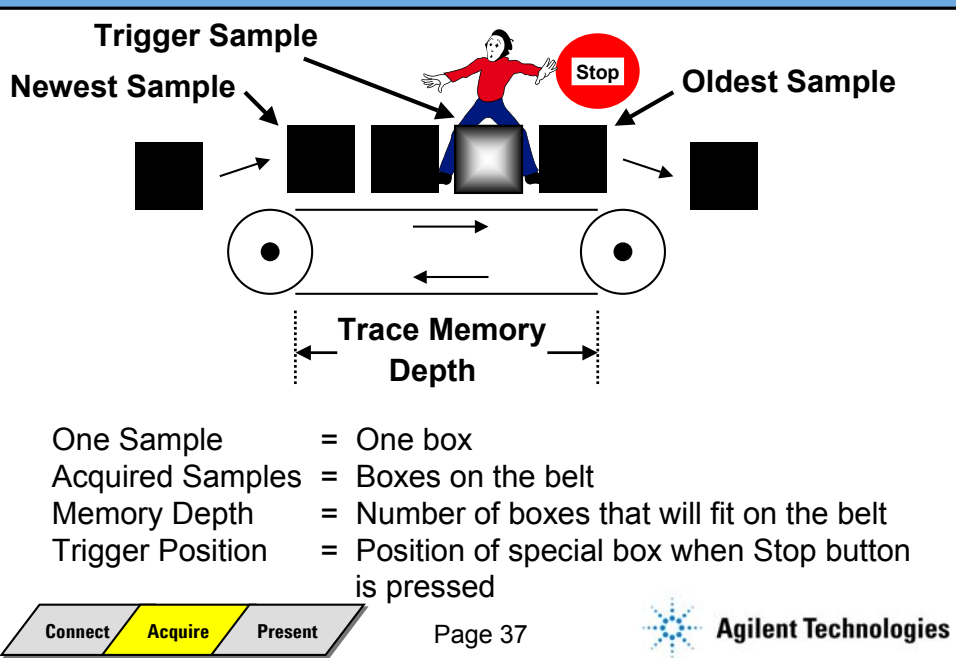Connect / **Acquire** / Present   Page 37   **Agilent Technologies**
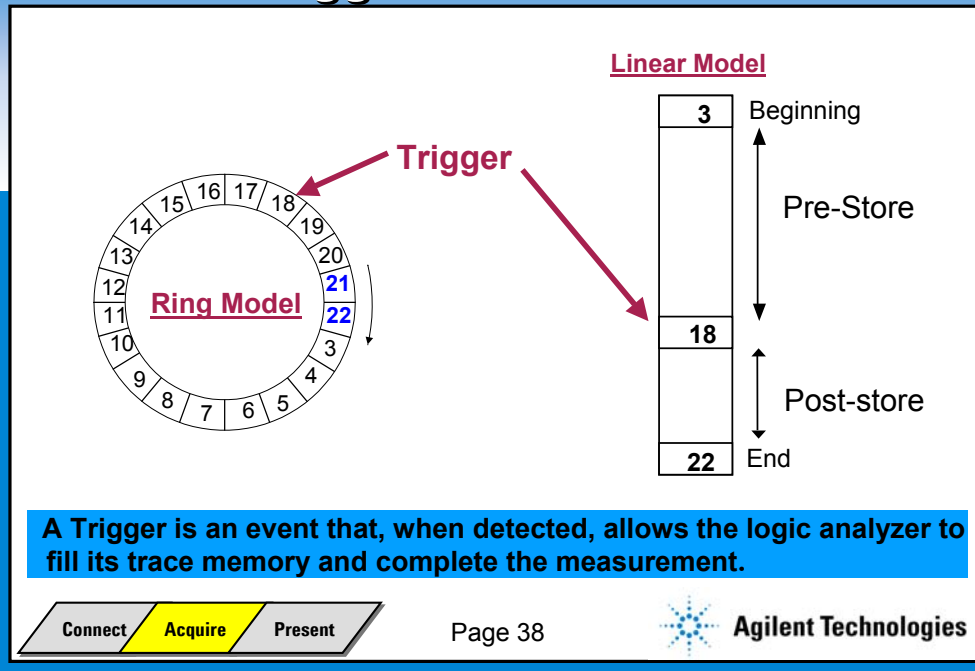
The memory of a logic analyzer can be compared to a very long conveyor Belt, and the samples acquired from the Device Under Test (DUT) as boxes on the Conveyor Belt. At one end, new boxes are placed on the conveyor Belt, and at the other end the boxes fall off.

In other words, because logic analyzer memory is limited in depth (number of samples), whenever a new sample is acquired the oldest sample currently in memory is thrown away if the memory is full.

In this mode the analyzer is storing all qualified samples in the trace memory. As the memory fills, older data will be overwritten. If you stop the analyzer before the trigger is found, you will see this pre-trigger storage.

What is a Trigger?

Linear Model

Ring Model

Trigger

Beginning

Pre-Store

Post-store

End

A Trigger is an event that, when detected, allows the logic analyzer to fill its trace memory and complete the measurement.

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The logic analyzer memory system is similar to a circular buffer. When the acquisition is started, the analyzer continuously gathers data samples and stores them in memory. When memory becomes full, it simply wraps around and stores each new sample in the place of the sample that has been in memory the longest.

New data is written over the oldest data until the specified post-store has been stored.

This process will continue until the logic analyzer finds the trigger point. The logic analyzer trigger stops the acquisition at the point you specify and provides a view into the DUT.

The primary responsibility of the trigger is to stop the acquisition, but it can also be used to control the selective storage of data.

Single-Shot View of System

Display Tool

Trace Memory

Trigger

Captured Activity
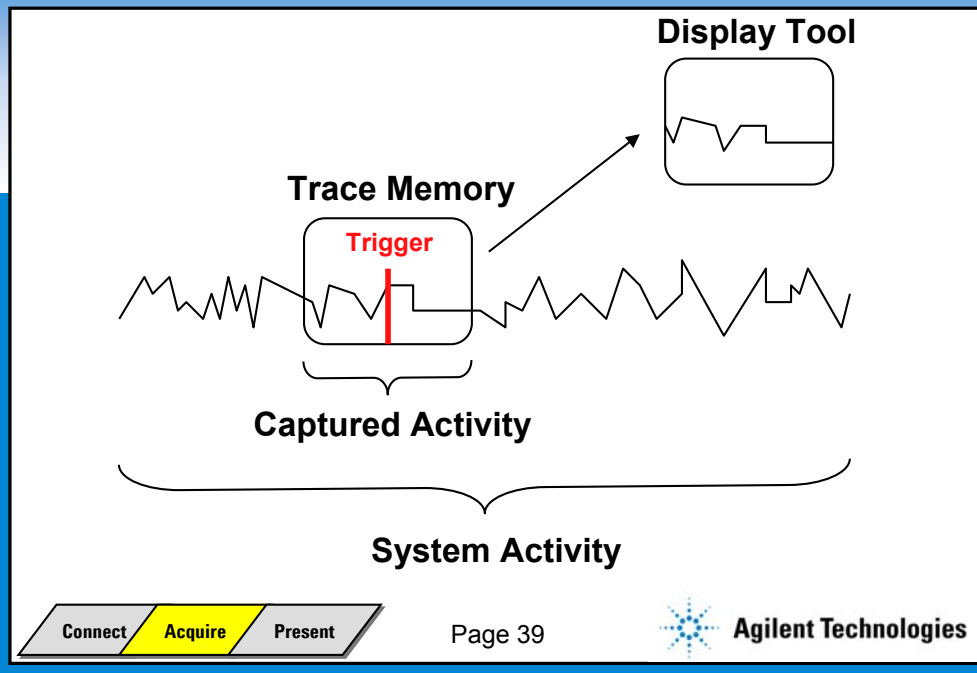
System Activity

Logic analyzers run in a single shot mode. They continually capture data until a trigger event. They then display the captured data to the screen. The logic analyzer shows one snap shot of the system activity.
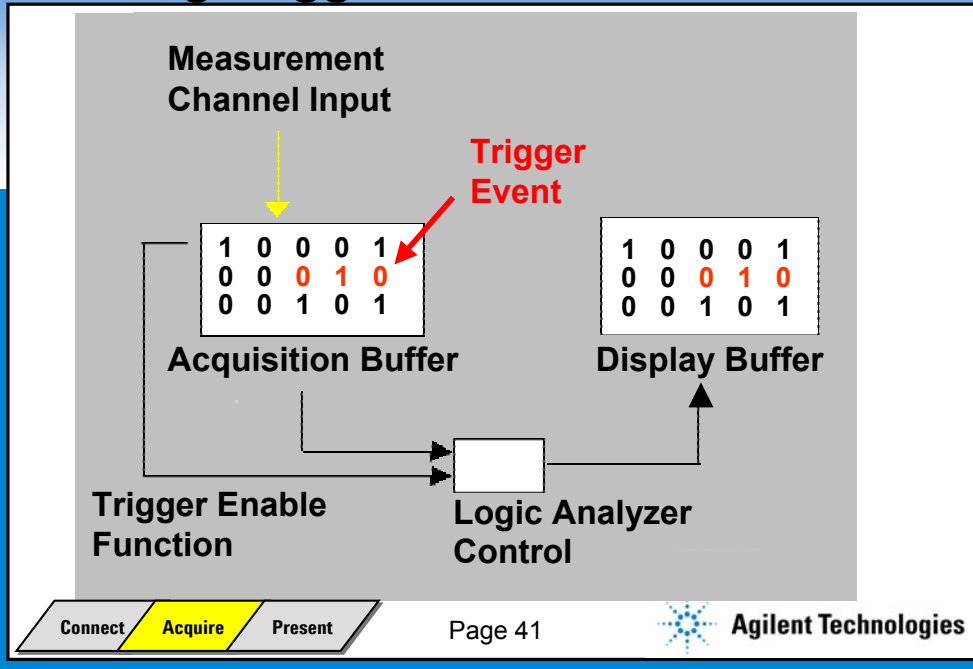
Trigger Positions

Options

Trigger Position - 50% poststore

|◄| [+] |►|

Acquisition Depth: 4M ▼
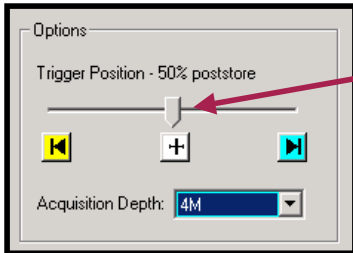
Trigger Position	Use of Trigger
Start	Observe code execution
Center (Default)	View time shortly before/after event
End	Trace cause of system halt Root cause analysis (uncorrelated symptoms)
0-100%	Variable, custom selection

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Defining Trigger Events

Measurement Channel Input

Trigger Event

```
1 0 0 0 1          1 0 0 0 1
0 0 0 1 0          0 0 0 1 0
0 0 1 0 1          0 0 1 0 1
```

Acquisition Buffer   **Display Buffer**

Trigger Enable Function   **Logic Analyzer Control**

Since digital circuits produce data continuously, the desired data must be isolated. This is accomplished by enabling the logic analyzer to recognize a trigger event—usually a distinctive data pattern.

The analyzer continuously stores data in an acquisition buffer while searching for the trigger event. Once the trigger event is found, [1] the logic analyzer transfers the contents of the acquisition buffer to the display buffer for display and examination.

Defining Simple Trigger Events

Trigger on Bus values

Bus/Signal	Simple Trigger
Sample Num	
My Bus 1	= , 8B
My Bus 1[0]	1
My Bus 1[1]	
My Bus 1[2]	
My Bus 1[3]	

Rising Edge
Falling Edge
Either Edge
Glitch
✓ High
Low
Dont Care

Advanced Trigger...

Overview   Waveform - 1

1

Trigger on Signal values

The analyzer's state specification menu can define a trigger event based on any address, data or control bus state condition. In this example, the logic analyzer stores all measured data until it detects the trigger event, [show 1] which is the address bus state of "043A."
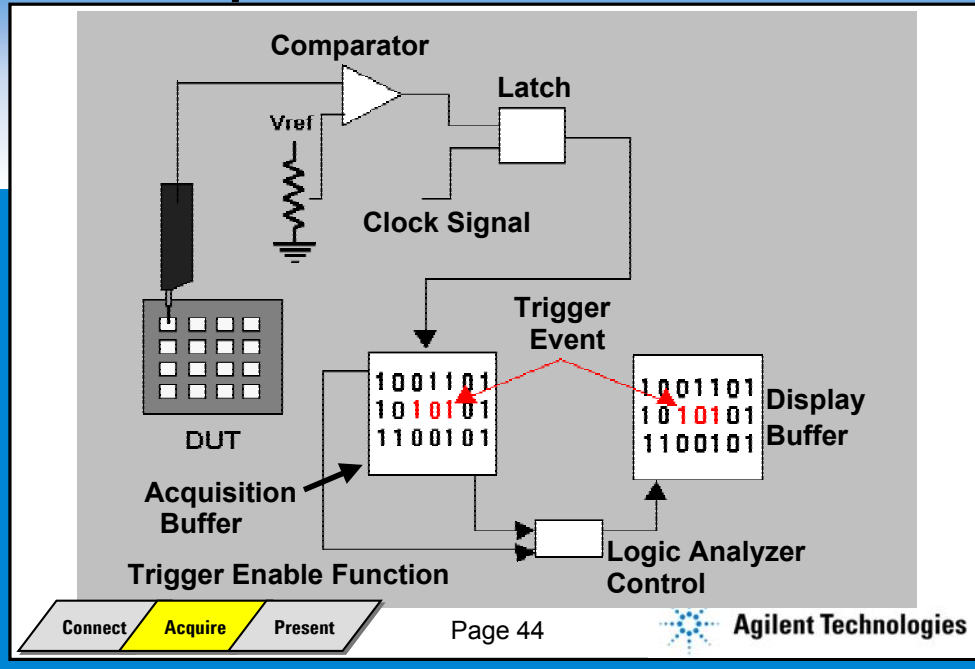
Defining Advanced Trigger Events
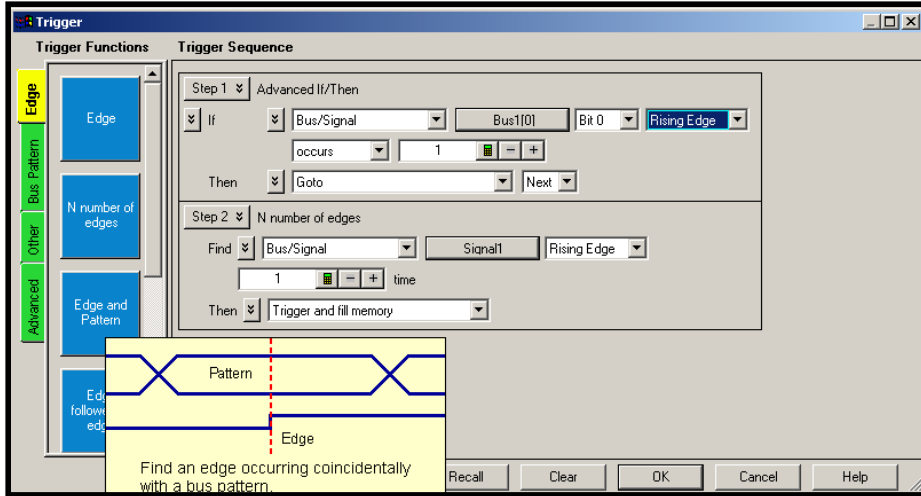
Upon finding the trigger event, the analyzer continues making measurements until the acquisition buffer is full. It displays the results with the trigger event in memory location +0000.

The Complete Measurement

The digitizing functions of comparing and clocking, combined with the control function of trigger enabling, provide all the capabilities needed for making a logic analyzer measurement. To complete the measurement, the contents of the display buffer are transferred to the logic analyzer screen for the user to view and analyze.

Displaying the Data

- **Waveform**
- **Listing**
- **Correlation to an Oscilloscope**
- **Inverse Assembly, Source Correlation**
- **Protocol Debug**
- **Eye Diagrams**

There are a number of ways to display the 1's and 0's to make sense of your digital design

Correlation to Oscilloscope
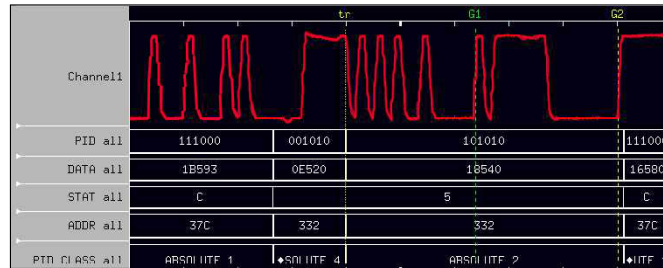
- **Import oscilloscope waveforms with time-correlated global markers**
- **Track errors through analog and digital**
- **Analyze analog characteristics of digital anomalies**

|				
Channel1				
PID all	111000	001010	101010	111000
DATA all	1B593	0E520	18540	16580
STAT all	C		5	C
ADDR all	37C	332	332	37C
PID CLASS all	ABSOLUTE 1	◆SOLUTE 4	ABSOLUTE 2	◆UTE 1

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If you require full logic analysis capabilities, but also require higher performance oscilloscope capabilities than are currently available in a standard logic-centric solution, then the Time Correlation Tool may be the best choice for your mixed analog & digital signal measurement applications. This type of solution is basically tying together a full-fledge logic analyzer with a full-fledge oscilloscope with a time-correlation fixture. On the surface you might think that this particular measurement solution has no compromises since each instrument has its own key contribution without compromises. Unfortunately, even this solution has its compromises. But let's take a look at the advantages first…

Correlation to Oscilloscope

Distorted D/A output as measured by scope module

5.00 MSa/s
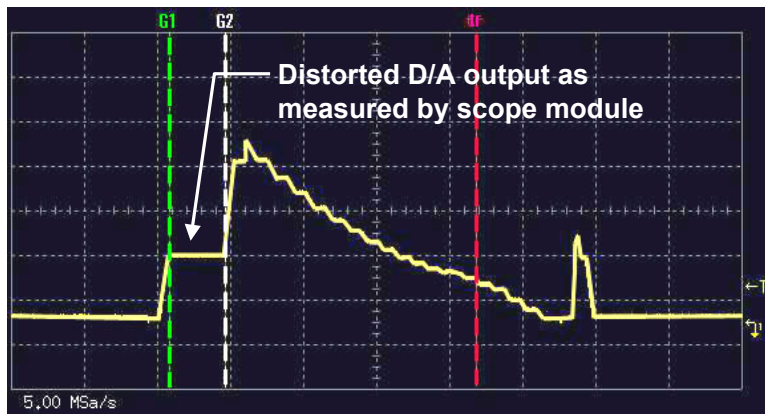
Scope triggered to find max distortion with G1 and G2 markers positioned at start and end of first flat distortion.

Analyzing the Digital-to-Analog Converter Output

When we take a closer look at the D/A converter's output using the logic analyzer's oscilloscope acquisition module, we occasionally see undesirable "flat-spots" on both the rising and falling edge of the triangular output waveform of the D/A converter. This is what is causing the intermittent "jerky" response of our mechanical output device. So, what is causing this intermittent problem?

The next step would be to set up a trigger condition that reliably catches only the "bad" output conditions. We can do this with a time-qualified trigger condition. We can now clearly see various flat distortions with every acquisition of the scope. We would now like to correlate this output condition with the controlling software. So, we should set up the global markets (G1 & G2) to bracket the longest flat distortion shown on screen.

Listing Correlated to Waveform at G1

PC	MPC821/860 Inverse Assembler
Symbols	10=hex, 10.=decimal, %10=binary

```
/q.elf:reset+0420    subi     r1 r1   0018
/q.elf:reset+0424    stmw     r26 0000(r1)
/q.elf:reset+0428    mfmsr    r26
/q.elf:reset+042C    ori      r26 r26 0002
/q.elf:reset+0430    mtmsr    r26
/q.elf:reset+0434    subi     r1 r1   0008
/q.elf:reset+0438    bl       q.:isr:ext_exception
G1  isr:ext_exception    mfspr    r0 lr
ext_exceptio+0004    stw      r0 0004(r1)
ext_exceptio+0008    stwu     r1 FFF8(r1)
ext_exceptio+000C    lis      r12 0000
```

State listing reveals code branching just prior to G1.

Listing Correlated to Waveform at G1

However, when we look at the state listing that is time-correlated with the scopes acquisition at the point of the first global marker (G1), we see that at this point the firmware exits execution of the D/A code, and then branches off to somewhere else. So, where does it go?

Interrupt Service Routine Source Code

```
53  void
54  ext_exception()  /* C Routine for Ext Interrupt
55  {
56      unsigned long exception;
57      unsigned short temp;
58
59      /* This is the C Routine to handle an exterr
60      /* This function is called by the extern_lov
61      /* located in file 'exc_table.s'.
62      /* Note that other external interrupts are c
63      /* this routine.*/
64
65      exception = quicc->sivec;
66
```

Between G1 and G2 D/A execution is interrupted when code goes to interrupt service routine. Line 55 correlated to G1 marker in state listing and waveform.

Interrupt Service Routine Source Code

Looking at the source code again, we can see that during code execution, the code branches off to a priority interrupt routine. So while this interrupt routine is being processed, naturally the output of the D/A converter stays flat at a constant DC level. Once the interrupt routine has finished processing (G2 marker), the D/A code continues to generate the desired analog ramping voltage.

Problem discovered! For smooth actuation of our embedded output device, the D/A converter needs to take priority over any interrupts. For the software/firmware designer, this should be an easy fix.

Protocol Analysis

- **Display parallel bus data at protocol level**

- **Protocol trigger macro allows easy trigger setup, eliminates manual configuration of complex measurements**

- **Time correlation with other system buses**

- **Coverage includes:**
  - **RapidIO**
  - **Utopia**
  - **POS-PHY 4 (SPI-4.2)**
 - **Serial ATA**
  - **Proprietary/Custom Protocols**

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Another addition to the logic analyzer's data views are the packet decoders for various protocol analysis needs. This moves beyond the traditional state Listing display and provides with the level of packet detail needed to gain insight from the data

Slide: **Eye Scan**

What is Eye Scan?

- **Provides signal integrity validation measurements of entire high-speed buses.**

- **Uses high resolution comparators to scan across specified time and voltage range.**

- **Provides up to 1mV and 10ps resolution.**

- **Can be used as a tool of "first attack" to reveal tough signal integrity problems.**
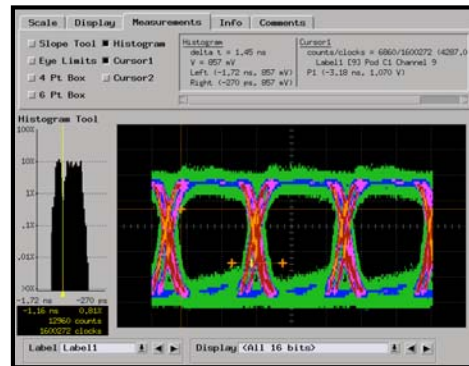
Connect / Acquire / **Present**   Page 51   **Agilent Technologies**

With Eye Scan in the logic analyzer, you can get a composite eye-diagram display of ALL signals on a bus for validation purposes. With a scope, you are limited to the number of channels of the oscilloscope.

The actual acquisition technique is very different from real-time oscilloscopes, but since eye-diagrams are fundamentally a repetitive measurement, the results are similar. With Eye Scan, high resolution comparators scan across a time and voltage range specified by the user with up to 1mV and 10ps resolution. This type of tool is ideal as a "first attack" approach for revealing tough signal integrity problems across an entire bus.

Eye scan is a great compliment to an oscilloscope. The logic analyzer will allow you to look at al of the channels simultaneously and identify where the problem signals are. From there, the scope can be used to determine the parametric characteristics of the bgtroublesome signal.

Summary

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Using a Logic Analyzer vs. an Oscilloscope

Use a Logic Analyzer to:	Use an Oscilloscope:
See many signals at once	To get precise time interval information
Look at signals the same way your hardware does (State Mode)	
Trigger on a pattern of highs and lows on several lines and see the result	To look at the analog characteristics of a signal
Verify timing relationships among several or hundreds of lines (Timing Mode)	

Connect / Acquire / Present

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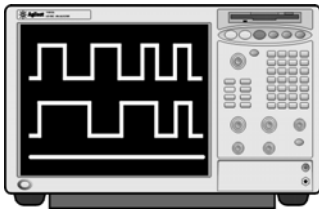**Agilent Technologies**

State vs. Timing

Timing Analysis
- When the event happened
- Edge relationships
- Hardware debug

State Analysis
- What event happened
- Monitor execution of processor
- Software and System Integration

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Multiple Views Provide the Right Level of Insight

System Performance

Eye Scan

Oscilloscope

Listing & IA

Waveform

Source Code

Packet Decode

Connect | Acquire | Present

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Agilent has always provided a variety of ways to view your data for analysis purposes. The traditional waveform and listing views, as well as the correlation to source code and oscilloscope views are still there. The Eye Scan and Packet Decode views we just discussed are simply new additions to the robust tools already available that extend your ability to analyze the data and gain quick insight.

Agilent Back to Basics eSeminars

Future Back to Basics eSeminars:

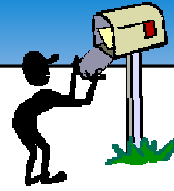- **RF Spectrum Analysis Basics – February 18th**

Recently Archived Back to Basics eSeminars:

- **Digitizing Oscilloscope Basics**
- **RF Network Analysis Basics**

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